**Subject: Computer Arch. Lab Stream: CSE**

**Course Code:** PCC-CS492

**Semester: Even Year of Study: 2020-21**

**After completion of this course the students will be able to**

|  |  |  |
| --- | --- | --- |
| **CO** | **Course outcome statements** | **Bloom’s Level** |
| 1 | Gain knowledge of hardware simulation for both structural and behavioral approach. | Synthesis |
| 2 | Design combinational systems composed of standard combinational modules, such as multiplexers, decoders etc. | Evaluation |
| 3 | Design sequential systems composed of standard sequential modules, such as counters and registers. | Analysis |
| 4 | Solve and Implement complex and new problems using modular approaches. | Comprehension |
| 5 | Test feasibility and functionality of both known and unknown problems. | Knowledge |
| 6 | CreateVerilog program to design a system. | Comprehension |

**PO Mapping with CO**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| 1 | 2 | - | - | - | - | - | - | - | - | - | - | 2 |
| 2 | 2 | 2 | 2 | - | - | - | - | - | - | - | - | 2 |
| 3 | 2 | 3 | 2 | 2 | - | - | - | - | - | - | - | 2 |
| 4 | 2 | 2 | 3 | 2 | - | - | - | - | - | - | - | 2 |
| 5 | 3 | 2 | 2 | 3 | 2 | - | - | - | - | - | - | 2 |
| 6 | 2 | - | - | - | - | - | - | - | - | - | - | 2 |
| Avg |  |  |  |  |  |  |  |  |  |  |  |  |

**PSO Mapping with CO**

|  |  |  |  |
| --- | --- | --- | --- |
| **CO** | **PSO1** | **PSO2** | **PSO3** |
| 1 | 2 | - | - |
| 2 | 2 | - | - |
| 3 | 2 | 2 | 2 |
| 4 | - | 2 | - |
| 5 | 2 | 2 | 3 |
| 6 | 2 | - | - |
| Avg |  |  |  |